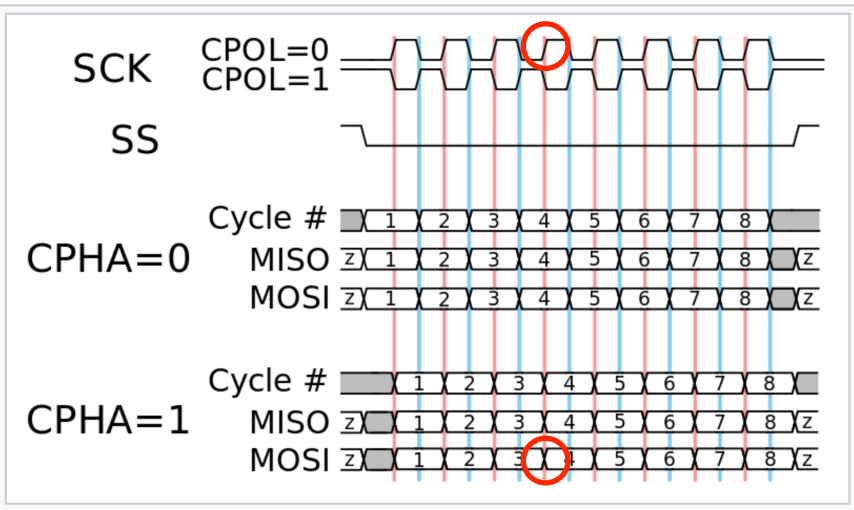
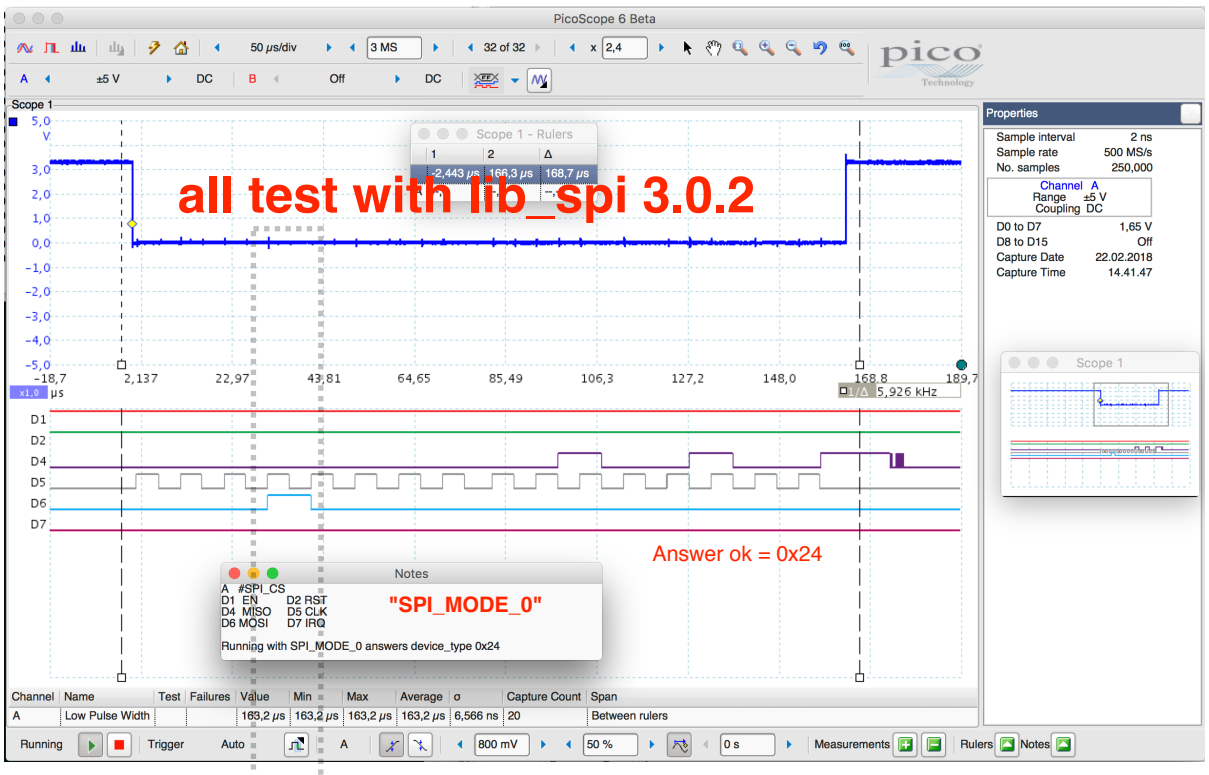
https://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus

Clock polarity and phase [edit]

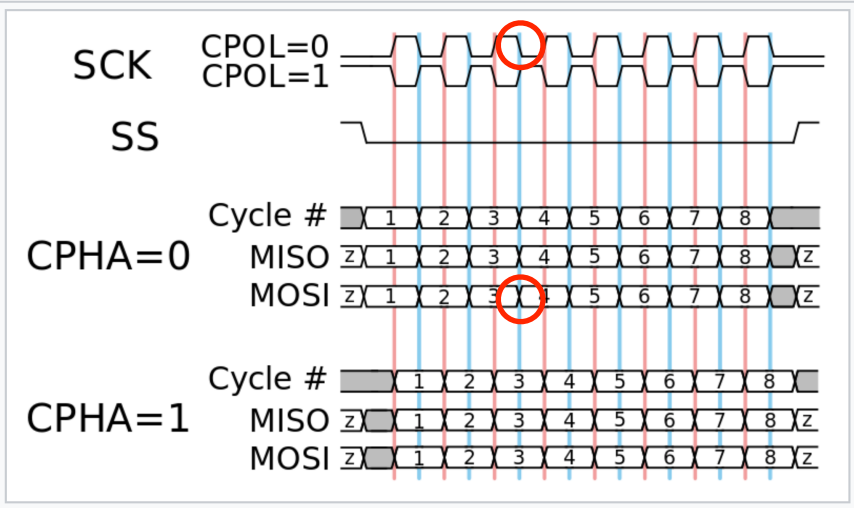


A timing diagram showing clock polarity and phase. Red lines denote clock leading edges, and blue lines, trailing edges.

XMOS behaves like MODE 1?

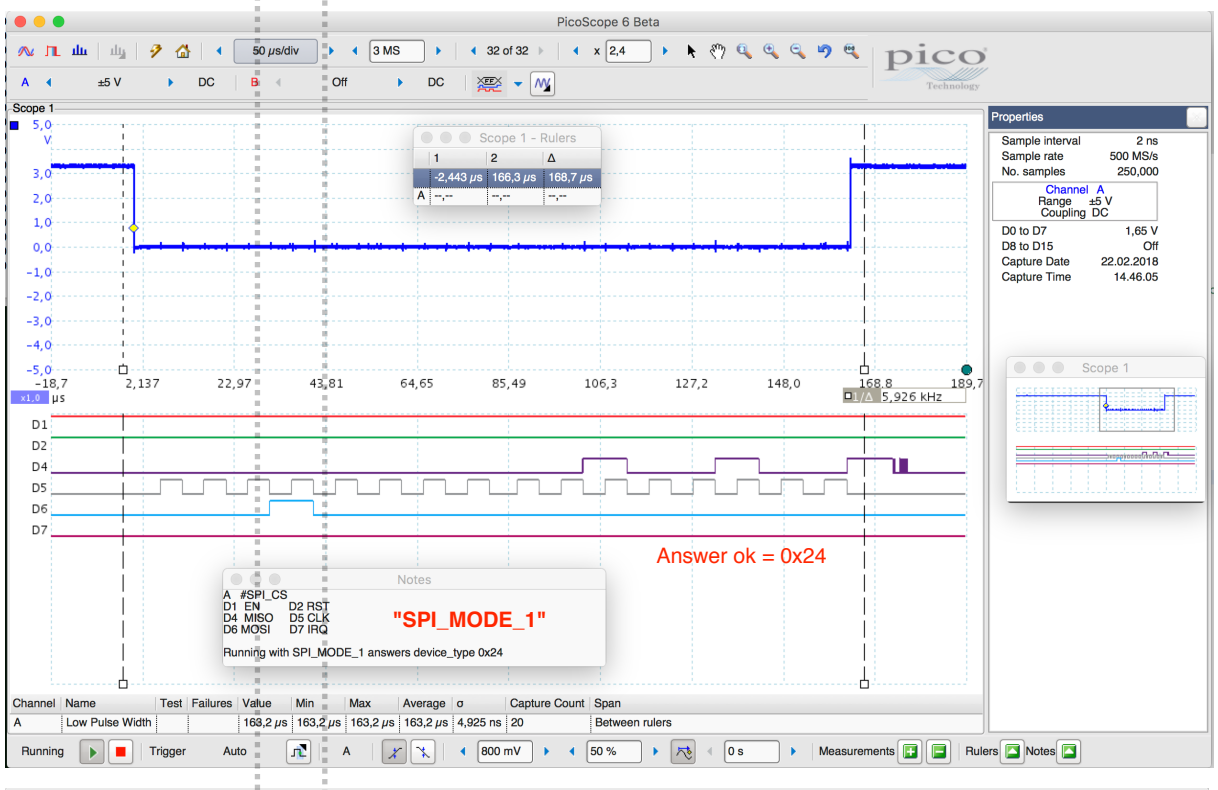


Clock polarity and phase [edit]

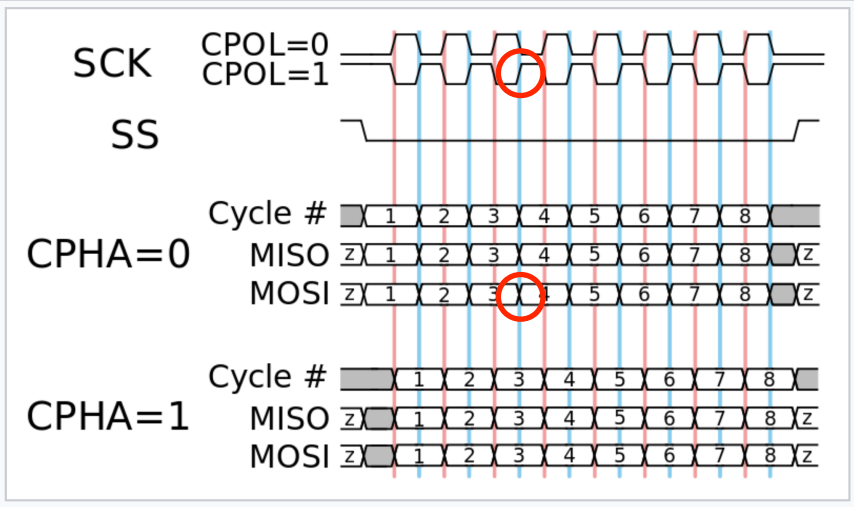


A timing diagram showing clock polarity and phase. Red lines denote clock leading edges, and blue lines, trailing edges.

XMOS behaves like MODE 0?

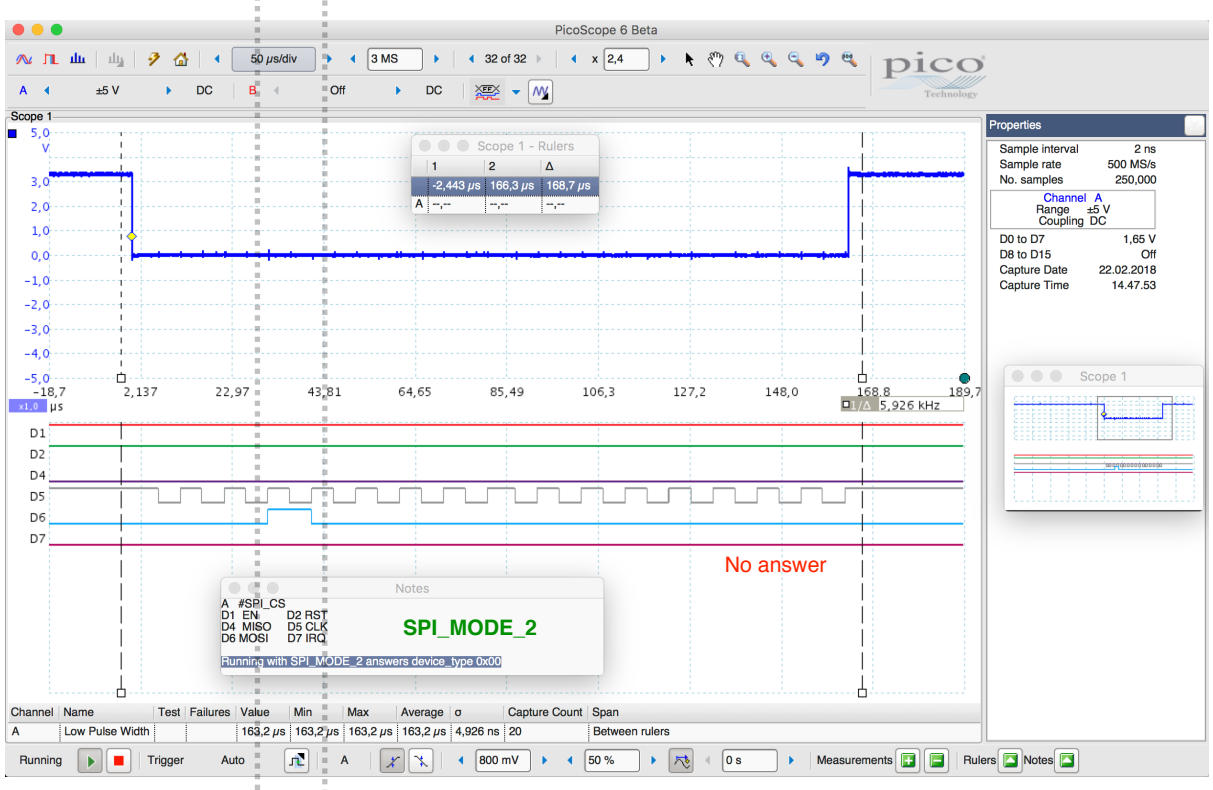


Clock polarity and phase [edit]

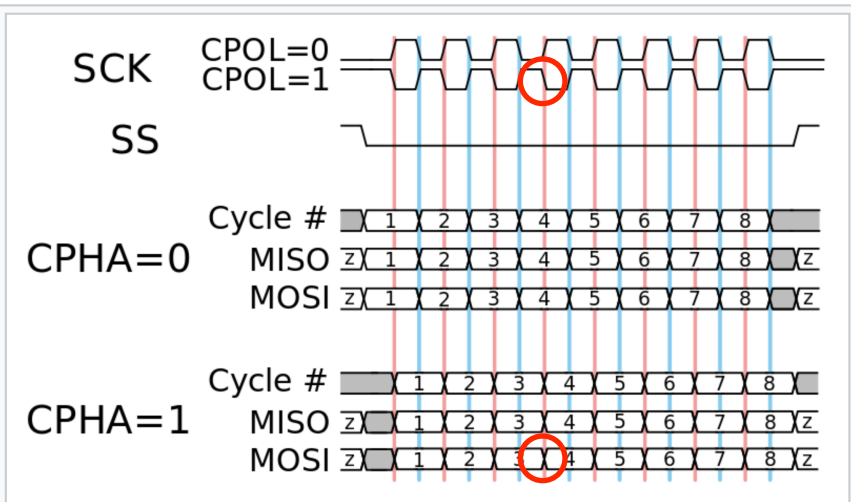


A timing diagram showing clock polarity and phase. Red lines denote clock leading edges, and blue lines, trailing edges.

XMOS behaves like MODE 2 (correct)

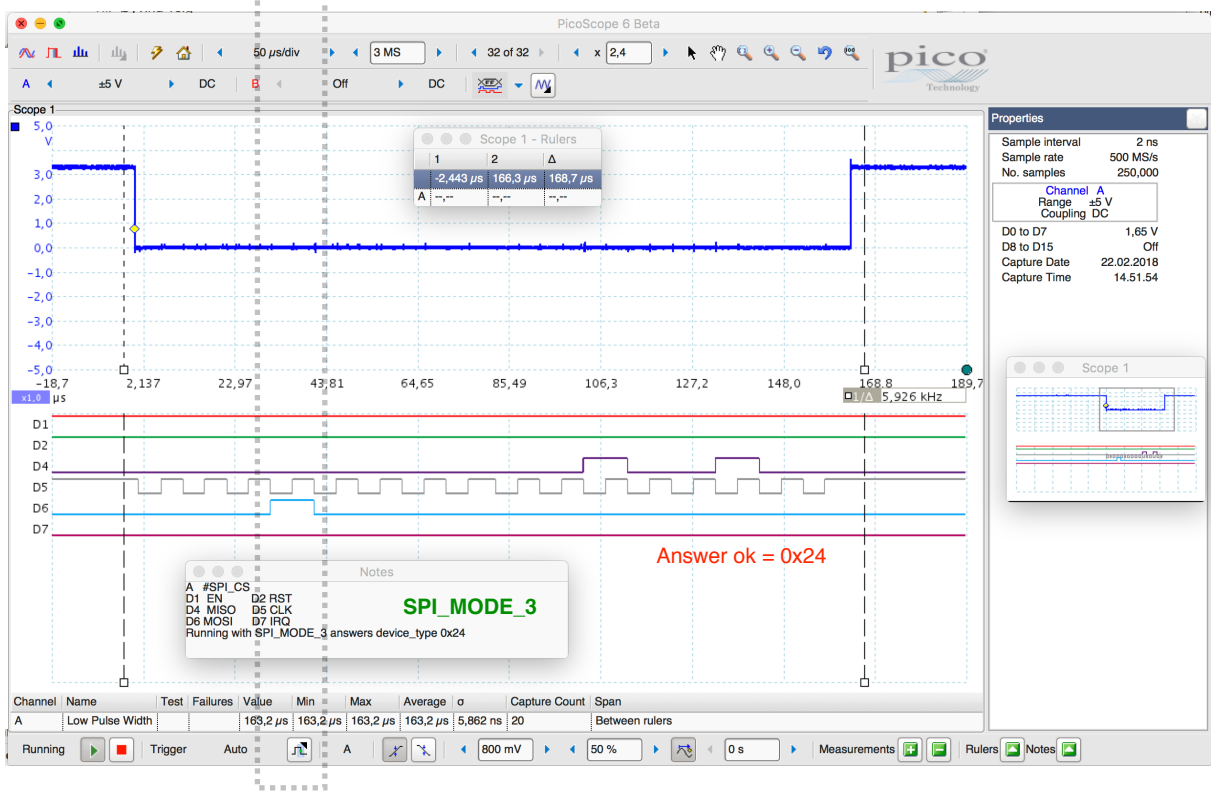


Clock polarity and phase [edit]



A timing diagram showing clock polarity and phase. Red lines denote clock leading edges, and blue lines, trailing edges.

XMOS behaves like MODE 3 (correct)



Measured by Øyvind Teig 22Feb2018, see http://www.teigfam.net/oyvind/home/technology/165-xc-code-examples/#lib_spi